REMARKS

Claim 1 was amended herein. It is respectfully submitted that the amendments to claim 1 do not add new matter and have adequate support throughout the Specification, for example, at paragraph 8 and Figures 3 and 4.

I. REJECTIONS OF CLAIMS 1-5, 10 AND 11 UNDER 35 U.S.C. § 102(e)

Claims 1-5, 10 and 11 were rejected under 35 U.S.C. § 102(e) as anticipated by U.S. Patent No. 6,754,116 to Janik et al. ("Janik"). Respectfully, Applicants traverse.

Janik relates to a testing circuit used testing multi-memory semiconductors. (Janik; Abstract). The testing circuit includes an integrated semiconductor circuit 1 including an on-chip test controller 4. (Janik; col. 7, lns. 52-54). The controller 4 includes a Built-In Self Test (BIST) processor 2, an additional processor 3 coupled to the BIST processor 2, a multiplexor (MUX) coupled to the BIST processor 2 and the additional processor 3, and memory banks A and B coupled to the MUX. (Janik; col. 7, ln. 55 to col. 8, ln. 3). An external lead 5 is provided for external test signals. (Janik; col. 8, lns. 11-12). According to Janik, "in each case only a single line [is] selected and the corresponding commands [are] forwarded to the memory banks A, B." (Janik; col. 8, lns. 11-12). In this manner, only one of the BIST processor 2, the additional processor 3, and the external lead 5 are connected to memory banks A and B at any given time.

This is in sharp contrast to claim 1, which recites a "muxing circuit . . . configurable to couple the first access device to the first memory bank and the second access device to the second memory bank ***simultaneously***, and . . . configurable to couple the second access device to the first memory bank and the first access device to the second memory bank ***simultaneously***." This simultaneous connecting ability is nowhere to be found in Janik.

For at least the foregoing reasons, it is respectfully submitted that claim 1 is allowable over Janik. Furthermore, since claims 2-5, 10, and 11 ultimately depend from claim 1, it is respectfully submitted that these claims are allowable over Janik for at least the same reasons. Accordingly, it is kindly requested that the rejections of claims 1-5, 10 and 11 under 35 U.S.C. § 102(e) be withdrawn.

II. REJECTIONS OF CLAIMS 6-9 UNDER 35 U.S.C. § 103(a)

Claims 6-9 were rejected under 35 U.S.C. § 103(a) as unpatentable over Janik in view of U.S. Patent No. 6,430,648 to Carnevale ("Carnevale"). Respectfully, Applicants traverse.

As described above with respect to the anticipation rejection of claim 1, Janik fails to discloses a "muxing circuit . . . configurable to couple the first access device to the first memory bank and the second access device to the second memory bank ***simultaneously***, and . . . configurable to couple the second access device to the first memory bank and the first access device to the second memory bank ***simultaneously***." Furthermore, any reading of Carnevale makes clear that this reference fails to cure the critical deficiencies of Janik as applied against claim 1. Since claims 6-9 ultimately depend from claim 1, it is respectfully submitted that these claims are allowable over Janik and Carnevale, considered individually or in combination.

For at least the foregoing reasons, it is kindly requested that the rejections of claims 6-9 under 35 U.S.C. § 103(a) be withdrawn.

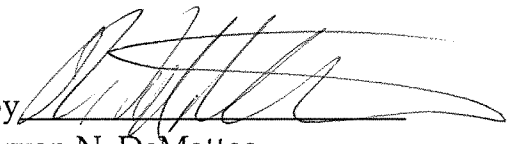
III. CONCLUSION

In view of the foregoing, reconsideration and allowance of claims 1-11 are solicited. Applicants believe the pending application is in condition for allowance.

Dated: XXXXXX

Respectfully submitted,

Dated April 2, 2007

By 

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